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10/669,852	09/25/2003	Toshiyuki Kasai	117024	4391

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EXAMINER
SHERMAN, STEPHEN G

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,852	KASAI, TOSHIYUKI	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14 and 17-29* is/are pending in the application.

4a) Of the above claim(s) *6,7,19,20 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-5, 8-14, 17-18 and 21-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 21 May 2007. Claims 1, 4-14 and 17-29 are pending, of which 6-7, 19-20 and 29 have been withdrawn from consideration.

Election/Restrictions

2. Newly submitted claims 6-7 and 19-20 and previously withdrawn claim 29 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Claims 6-7, 19-20 and 29 are drawn to Figure 5, whereas claims 1-28 are drawn to Figure 3. The inventions shown in Figure 3 and Figure 5 are directed to related species. The related inventions are distinct if the (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant case, the inventions as claimed cannot be used together since they are different circuit structures for pixels, and therefore are not capable of being used together.

Furthermore, the inventions as claimed do not encompass overlapping subject matter and there is nothing of record to show them to be obvious variants.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 6-7, 19-20 and 29 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

3. Applicant's election with traverse of the originally presented claims in the reply filed on 21 May 2007 is acknowledged. The traversal is on the ground(s) that claims 1-5, 7-18 and 20-28 are generic to both species and that since these claims have been examined, the examiner should examiner all of the claims. This is not found persuasive because claims 1-5, 8-18 and 21-28 are NOT generic. Independent claims 1 and 14 are specifically drawn to the invention of Figure 3. The claims state that there is a first and second circuit and that these circuits make a current mirror circuit. Figure 5, however, only has ONE circuit, not a first and a second, and there is NO CURRENT MIRROR in Figure 5. Therefore, claims 1-5, 8-18 and 21-28 are NOT generic. Thus, both species were NOT examined and the restriction is proper.

The requirement is still deemed proper and is therefore made FINAL.

Response to Arguments

4. Applicant's arguments filed 21 May 2007 have been fully considered but they are not persuasive.

The applicant argues starting on page 13, last paragraph, the objection made to claims 1, 5, 14 and 18 because the feature "at least one of the first circuit unit and the second unit including a plurality of transistors connected in series or in parallel," was not supported by Figure 3. The applicant states: "It is not necessary, in order to satisfy any formal requirement, that every varying embodiment be specifically depicted in a figure. The examiner respectfully disagrees.

While the examiner understands that the claims when ready broadly could be supported by Figure 3, but the remarks and amendments made by the applicant indicate that it is intended by the applicant that the first circuit can be in series and that the second circuit can be in parallel, which brings up the 112, 1st paragraph rejection with respect to the newly amended claim 5. Thus, it is clear the applicant wants claim 1 to encompass that feature which is not supported by the specification. Thus the objection is maintained.

Claim Objections

5. Claims 1 and 14 are objected to because of the following:

The claims recite the limitation "at least one of the first circuit unit and the second circuit unit including a plurality of transistors connected in series or in parallel." Figure 3, however, only shows that the first circuit unit containing transistors connected in parallel and the second circuit unit containing transistors connected in series. Therefore, based

on the wording of the claim limitation, at least one of the first and second circuit units has transistors in series or parallel, however, the specification does not allow for the choice between parallel or series. For example, if the examiner chose the second circuit unit, the limitation would require it to have transistors in either parallel or series, but Figure 3 shows only the second circuit having transistors in series and therefore having them in parallel has not been disclosed as an option and cannot be claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 5 and 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 5 and 18 recite that the first circuit unit includes a plurality of transistors connected in series, and the second circuit unit includes a plurality of transistors connected in parallel, which is not enabled by the specification. The specification, such as in Figure 3, only shows that the first circuit 40 is in parallel and the second circuit 30

is in series. Furthermore, the specification only explains the connections with respect to Figure 3. There is no support for the first circuit 40 to be in series or for the second circuit 30 to be parallel anywhere in the specification.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 14 both recite: "at least one of the first circuit unit and the second circuit unit includes a plurality of transistors connected in series or in parallel" then states: "each of the first circuit unit and the second circuit unit having the plurality of transistors having the same driving capability." This is indefinite because it is unclear whether the applicant wants both of the first and second circuit units to have a plurality of transistors each with the same driving capability or whether only the circuit unit having the plurality has the same driving capability. Also the claim is indefinite because the claims states that at least one of the first and second circuit units has a plurality, then the claim states that each has THE plurality. This makes it unclear to the examiner as to how each of the first and second circuit units can have the same plurality of transistors.

For the purposes of examination, the examiner will consider claims 1 and 14 to have been meant to be claims consistent with Figure 3 of the specification, where the both of the first circuit unit and the second circuit unit have a plurality of transistors.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 1, 4-5, 8-14, 17-18 and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,909,242) in view of Yumoto (US 2005/0200300).

Regarding claims 1, Kimura discloses an electronic circuit, comprising:

a first circuit unit (Figure 19, transistor 1907) through which a first current having a first current level passes (Figure 20A shows that current I_2 flows through transistor 1907.);

a capacitor element (Figure 19, item 1909) to store a quantity of electric charge corresponding to the first current level (Column 6, lines 25-53 explain that electric charge stored in the capacitor is equal to I_2 at the end of the charging procedure [towards the end of the passage].);

a second circuit unit (Figure 19, transistor 1908) to generate a second current having a second current level different from the first current level on the basis of the quantity of electric charge stored in the capacitor element (Figure 20C shows I_{EL} that flows through transistor 1908, where the current level will be different based upon the specifications of the transistors 1907 and 1908 as explain in column 6, lines 62-67.), and

the first circuit unit and the second circuit unit constituting a current mirror circuit (Column 6, lines 57-58).

Kimura does not explicitly teach that the first circuit unit of Figure 19 includes a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected.

However, Kimura does teach a plurality of transistors connected in parallel, respective gates of the transistors being mutually connected (Fig. 27B, see column 43, lines 27-35, and see column 43, lines 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the parallel transistors of Kimura into the first circuit of Kimura's embodiment in Figure 19 in order to have a method of further limiting possible display irregularities from developing.

Kimura fails to teach that the second circuit unit includes a plurality of transistors connected in series with respective gates of the second circuit unit transistors being mutually connected, and also fails to teach the plurality of transistors having the same driving capability.

Yumoto discloses of a second circuit unit that includes a plurality of transistors connected in series with respective gates of the second circuit unit transistors being mutually connected (Figure 8 shows a second circuit made up of TFT2a and TFT2b, where the gates are connected and the transistors are in series.)., the plurality of transistors having the same driving capability (Paragraph [0027] explains that the transistors have the same driving capability, i.e. W1 and W2 are set equal, L1 and L2 are set equal, and Idrv/Iw=1, which means that the driving capability is the same. The paragraph also states that the same TFTs can be used for each TFT. Thus, each TFT would be the same and each TFT would thus have the same driving capability.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention wad made to make the second circuit taught by Kimura have two transistors connected in series as taught by Yumoto in order to suppress the leakage current which forms when having only one transistor such that display defects can be prevented (See paragraph [0073] of Yumoto.).

Regarding claims 4 and 17, please refer to the rejection of claim 1.

Regarding claim 14, please refer to the rejection of claim 1, and furthermore Yumoto also discloses and electronic device provided with a first signal line (Figure 2, scan1), a second signal line (Figure 2, data), and a plurality of unit circuits (Figure 2, 25 PIXELs), each of the plurality of unit circuits comprising:

a switching elements connected to the first signal line (Figure 8 shows TFT3), and on/off state of the switching element being controlled by switching signals supplied from the first signal line (Figure 8 shows that the gate of TFT3 is controlled by scanA.);

a first circuit unit connected to the second signal line (Figure 8 shows that TFT1 is connected to the line data through TFT3.), a first current having a first current level supplied from the second signal line passing through the first circuit unit by switching on the switching element (Paragraph [0065] explains that current level I_w passes through TFT1, where I_w is seen in Figure 8 to be flowing from the data line.); and

a capacitor and second circuit unit as described in the rejection of claim 1 (see Figure 8).

Regarding claims 8 and 21, Kimura and Yumoto disclose the electronic circuit and device according to claims 1 and 14.

Yumoto also discloses where the plurality of transistors being formed in a bundle (Figure 8, where the transistors here are considered "bundled" since they are close together).

Regarding claims 9 and 22, Kimura and Yumoto disclose the electronic circuit and device according to claims 1 and 14.

Yumoto also discloses where the first current level is higher than the second current level (Paragraph [0069] explains of an example where I_w is higher than I_{drv}.).

Regarding claims 10 and 23, Kimura and Yumoto disclose the electronic circuit and device according to claims 1 and 14.

Yumoto also discloses where the second current level is higher than the first current level (Paragraphs [0068]-[0069] explain that the values W1, W2, L1 and L2 can be chosen, meaning that these values can be chosen to make a case where I_w is lower than I_{drv}, therefore making the second current higher than the first.).

Regarding claims 11 and 24, Kimura and Yumoto disclose the electronic circuit and device according to claims 1 and 14.

Yumoto also discloses where there are electronic elements being supplied with the second current (Figure 8 shows the electronic element OLED).

Regarding claims 12 and 25, Kimura and Yumoto disclose the electronic circuit and device according to claims 11 and 24.

Yumoto also discloses where the electronic elements is an electro-optical element or a current-driven element (Paragraph [0067], at the end explains that OLED is current driven.).

Regarding claims 13 and 26, Kimura and Yumoto disclose the electronic circuit and device according to claims 12 and 25.

Yumoto also discloses where the electronic element is an organic EL element (Paragraph [0064] explains that the light emitting element is made of an organic EL element.).

Regarding claims 27 and 28, Kimura and Yumoto disclose an electronic apparatus having mounted therein the electronic circuit and device of claims 1 and 14 (Figure 2 of Yumoto shows that all circuits and devices, shows as PIXEL 25, are mounted in the display, also see paragraph [0001].).

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

18 June 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER